What is claimed is:

1. A method of forming a bonding pad of a semiconductor device comprising:

forming a first insulating layer over a semiconductor substrate;

forming a trench by removing some part of the first insulating layer;

forming a top metal interconnect in the trench;

forming a second insulating layer over the substrate including the top metal interconnect;

forming a contact hole by removing some part of the second insulating layer, the contact hole exposing a portion of the top metal interconnect;

forming a metal layer on the surface of the second insulating layer and the sidewalls and bottom of the contact hole;

forming a metal pad by removing some parts of the metal layer;

forming a third insulating layer over the second insulating layer and the metal pad; and

exposing the metal pad on the second insulating layer by removing some part of the third insulating layer.

- 2. The method as defined by claim 1, wherein the top metal interconnect is formed of copper using at least one of electroless plating and electroplating.
- 3. The method as defined by claim 1, wherein the first insulating layer is formed of at least one of SiO₂, FSG (fluorinated silica glass), and an insulating material with a low dielectric constant less than 3.0.
- 4. The method as defined by claim 1, wherein the second insulating layer is formed of at least one of SiO₂, TEOS (tetraethyl orthosilicate), and SiN.

- 5. The method as defined by claim 1, wherein the third insulating layer functions as a passivation layer.
- 6. The method as defined by claim 1, wherein the third insulating layer is at least one of a single layer and a multi-layer structure.
- 7. The method as defined by claim 6, wherein the single layer structure is formed of silicon nitride and the multi-layer structure is formed of oxide and nitride.